CMOS
Solid-State Photomultiplier

SSPM

Medical Imaging

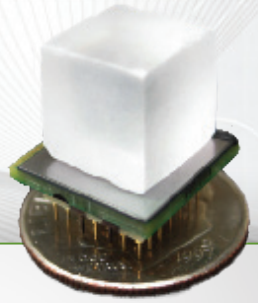
Dosimetry

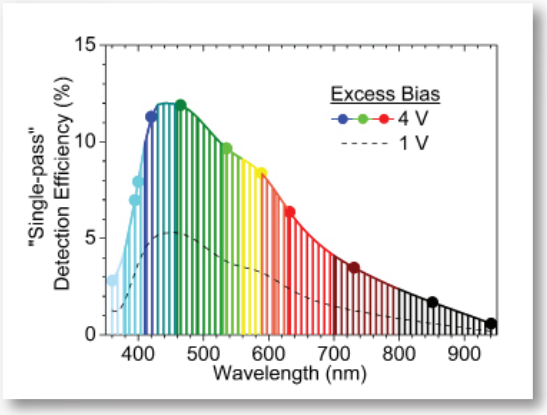
Spectrometry

The Science Behind the Technology

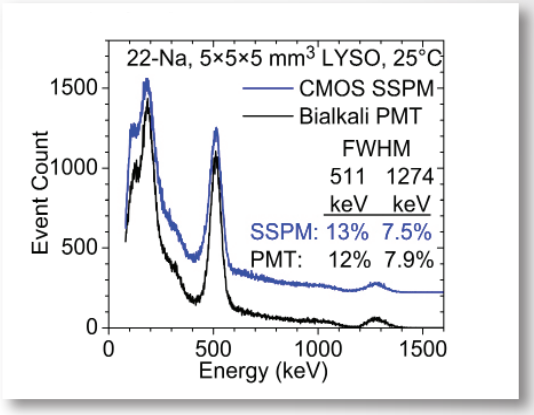
RMD
A Dynasil Company

CMOS
Solid-State Photomultiplier





Detection Efficiency (DE vs. Wavelength)



Gamma-Ray Spectrum
(LYSO Scintillator on PMT vs. an SSPM)

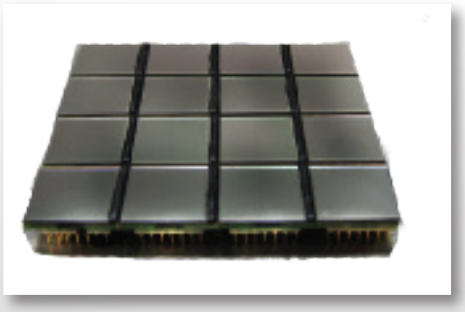
SSPM

The Perfect Replacement for PMT. CMOS Features Include:

- Independent readout of each sub-array.
- Completely protected; scintillator mount-ready.
- Tiling is possible without custom design using the chip-scale packaging.
- One silicon die per device, minimizing dead space between die when tiling.
- Energy resolution with LYSO Scintillator on 1 cm² SSPM is 13% at 511 keV.

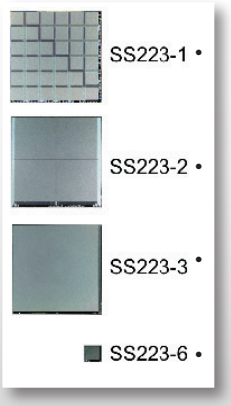
A solid-state, single photon-sensitive optical sensor. Optimized for pulsed, low-light applications at room temperature, such as:

- Scintillator Readout (Radiation Detection)
- Luminescence Sensors
- Stand-off Gamma-Ray Imaging
- Medical Imaging
- Dosimetry
- Laser-Induced Breakdown Spectroscopy (LIBS)
- Spectrometry



4 x 4 Array of 1cm x 1cm SS223-2 chips
(4 Arrays = 1 SSPM)

Available SSPM Chips



- SS223-1 • 6cm x 6cm array of 1.5mm x 1.5mm SSPMs
- SS223-2 • 2cm x 2cm array of 5mm x 5mm SSPMs
- SS223-3 • 1cm x 1cm array of 1.5mm x 1.5mm SSPMs
- SS223-6 • 1cm x 1cm array of 1.5mm x 1.5mm SSPMs

www.rmdinc.com info@rmdinc.com 617.668.6801

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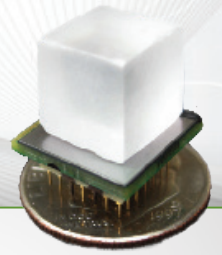

SSPM

Design	SS223-1CS12	SS223-2CS12	SS223-3CS12	SS223-6SQ4
Pixel Size	30 µm × 30 µm			
Array Format	6 × 6	2 × 2	1 × 1	1 × 1
Number of Pixels per Array	1156	12882	38416	1024
Array Fill Factor, FF	46%	46%	33%	46%
Array Area	1.5 mm × 1.5 mm	5.0 mm × 5.0 mm	10 mm × 10 mm	1.5 mm × 1.5 mm
Die Size	11 mm × 11 mm	11 mm × 11 mm	11 mm × 11 mm	1.9 mm × 1.8 mm
Packaging Options (see below)	49-pin PGA-CS	49-pin PGA-CS 32-pin B2B	49-pin PGA-CS 32-pin B2B	QFN
Wavelength of Max DE	450 nm			
Range of Operation	27.5 V – 32.5 V			
Pixel Capacitance	130 fF			
Array Capacitance	0.15 nF	1.7 nF	4.9 nF	0.15 nF
Recharge Time	30 ns			
Breakdown Voltage	27.2 +/- 0.2 V			
Temperature Coefficient on Breakdown	50 mV/°C			
Suggested Room Temperature Bias[2]	31.2 V			
DE_{max} for Array[3]	12%			
Gain	3×10^6			
Typical Dark Current at 25 °C for Array (Output Referenced)	18 µA	200 µA	600 µA	18 µA
Dark Count Rate per Pixel	~16 kHz			
Excess Noise Factor	~1.2			

PACKAGING OPTIONS:

- 49-pin PGA-CS: Fine pitch pin grid array with a chip-scaled substrate (pictured). Convertible to a BGA.
- 32-pin B2B.: Board to board connector with a chip-scaled substrate
- QFN: Commercially available quad-flat non-leaded plastic package.

NOTE:

Bias for bias-dependent parameters is highlighted in blue.

DE_{max} is a product of the QE, fill factor, and Geiger probability. After-pulsing and cross-talk were corrected before reporting.